REMARKS

Attached hereto is a marked-up version of the changes made by the current amendment captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Applicants thank the Examiner for the interview. Claims 1 – 14 and 16 remain in the application. Amendments have been made to claims 1, 5, 6, 12, and 16 to correct certain informalities for clarification purposes. No new matter has been included thereby.

Claims 1 – 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI ERA: Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322. The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory. Wolf is indicated as suggesting adjustment of threshold voltage using ion implantation. Lin et al. and Wolf were combined for the rejection. Applicants respectfully disagree.

In particular, Lin et al. and Wolf failed to show or suggest the claimed combination of elements for fabricating a flash memory device including an array of split gate cells recited in claim 1. Claim 1 recites providing a silicon substrate having a top surface and forming a common source region in an area of the top surface for each pair of the cell. The invention of claim 1 also includes implanting ions into predefined areas of each the common source region and forming floating gates associated with the cells, which has a substantial portion thereof overlying one of the predefined areas, which are not taught by Lin et al. In contrast, Lin et al. uses a completely different sequence of steps. Column 6 lines 26 – 28 of Lin et al. clearly illustrates that "..., In the present invention, however, source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." As noted above, the present invention implants ions into predefined areas of each common source region and forms floating gates associated with the cells. Implantation is provided before forming the gates. There are many other differences between Lin et al. and claim 1.

The present invention also includes forming select gates each having a first extremity extending over at least a portion of one of said floating gates and forming drain regions associated with each cells. Each of the drain regions is positioned proximate a second extremity of one of the select gates. The step of implanting ions into each of the predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

Clearly, Lin et al. fails to show or suggest the claimed combination of elements including implanting ions to provide the high coupling ratio for the associated flash cell as recited in claim 1. Rather Lin et al. taught a completely different technique for providing a high coupling ratio. Here, Lin et al. provides an increased coupling ratio by the introduction of a third polysilicon layer such that this additional poly line, through side-wall coupling, shares the voltage between the source and the floating gate (Col.1, lines 25 – 8, Col. 3, lines 57 – 61, Col. 4, lines 53 – 55, Col. 5, lines 21-25, Col 5, line 31 – 33). Here, the present invention provides the high coupling ratio without the need for the cost and complexity of adding an additional polysilicon line, as taught by Lin et al. Accordingly, Lin et al. fails to show or suggest the claimed element of implanting ions to provide the high coupling ratio for the associated flash cell. Wolf also fails to show or suggest the combination of elements including the claimed implanting process. Accordingly, claim 1 is patentable over the cited references.

Dependent claims 2–13 that are dependant from claim 1 are also patentable. The dependent claims are at least patentable for the reasons given above. Here, Lin et al. and Wolf do not show or suggest the combination of elements included in claims 2 – 13 when combined with independent claim 1. These claims are also patentable for other reasons.

In particular, claim 3 is patentable over the cited art. Claim 3 further recites that the ions implanted to form the common source region include arsenic ions. In rejecting claim 3, the Examiner suggested that although Lin et al. disclose (Col.6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used, and it would be obvious to one of ordinary skilled in the art to use an

arsenic implant instead of phosphorus, since both would produce similar results. The Applicants respectfully disagree. As noted earlier, Lin et al. suggests an additional polysilicon line to increase the coupling ratio (Col.1, lines 25 – 8, Col. 3, lines 57 – 61, Col. 4, lines 53 – 55, Col. 5, lines 21-25, Col 5, line 31 – 33), which has nothing to do with the present invention. The additional poly line is generally needed in Lin et al. because the coupling from the overlap of floating gate and the source region is limited by the extent of side diffusion of the source implant. Lin at al. suggests (Col. 6 lines 42 – 44) "Source implant is accomplished, **preferably**, by using phosphorous ions...," which is provided after forming the gates. Lin et al. relies upon phosphorous because the fast diffusion of phosphorous is needed for side diffusion for coupling the floating gate to the applied voltage of source region. The drawback of the approach suggested in Lin et al. is that the fast phosphorous diffusion will result in deeper source junctions leading to large cell size and poor device performance. In the present invention, the floating gate is formed after the source implant, and the overlap between the floating gate and the source region can be adjusted to increase the coupling ratio between the floating and the source region. Thus a higher coupling ratio can be provided as compared to the coupling ratio obtainable from the side diffusion of source implant. Therefore, deep and sideway diffusion in the source region is not needed for the coupling between the floating gate and the source region. As a result, the source junction can be made shallow by using the claimed arsenic implant instead of phosphorous to reduce cell size and improve device performance. The invention of Lin et al. and Wolf clearly failed to show or suggest claim 3 which recites that the ions implanted to form the common source region include arsenic ions. Accordingly, claim 3 is patentable over the cited references.

Claims 14 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al. The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory as recited in the instant application. Again, Applicants respectfully disagree.

In particular, Lin et al., Wolf, Mizuno et al., and Wilson et al. failed to show or suggest the claimed combination of elements for fabricating a flash memory

device having a high coupling ratio recited in claims 14. Claim 14 recites providing a silicon substrate, forming a sacrificial oxide layer, patterning a photoresist layer disposed over the sacrificial oxide layer to substantially define a source region of the substrate, implanting first ions into the substrate to form a common source region of the substrate using the patterned photoresist layer as an implant mask, removing the patterned photoresist layer and the sacrificial oxide layer to expose the top surface of the substrate, forming a tunneling oxide layer over the exposed top surface of the substrate, and depositing a first polysilicon layer over the tunneling oxide layer. The invention of claim 14 also includes depositing a nitride masking layer over the first polysilicon layer, patterning and etching the nitride masking layer to expose first portion and second portion, the first and second exposed portions defining first and second floating gate regions. In contrast, Lin et al. uses a completely different sequence of steps. Column 6 lines 26 – 28 of Lin et al. clearly illustrates that "...In the present invention, however, source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E. ..." As noted above, the present invention implants ions into predefined areas of each the common source region and then forms floating gates associated with the cells. Implantation is provided before forming the gates, and the overlap between the floating gate and the source region can be adjusted to increase the coupling ratio between the floating and the source region. Thus a higher coupling ratio can be provided as compared to the coupling ratio obtainable from the side diffusion of source implant. As noted earlier, Lin et al. suggests an additional polysilicon line to increase the coupling ratio (Col.1, lines 25 – 8, Col. 3, lines 57 – 61, Col. 4, lines 53 – 55, Col. 5, lines 21-25, Col 5, line 31 – 33), which has nothing to do with the present invention. There are many other differences between Lin et al. and claim 14.

Claim 14 of the present invention also includes implanting second ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of the common source region, in order to adjust the threshold voltage of the flash memory device.

The invention of claim 14 further includes forming a floating gate oxide, removing the nitride masking layer; etching the first polysilicon layer and the tunneling oxide layer using the floating gate oxide layer as a mask leaving remaining portions of the first polysilicon layer and the tunneling oxide disposed beneath the floating gate oxide layer, and exposing a portion of the substrate, each the remaining portion of the first polysilicon layer forming a floating gate having side walls, having a portion which overlies a portion of the common source region thereby providing a high coupling ratio for an associated cell. As discussed earlier, the overlap between the floating gate and the source region can be adjusted to increase the coupling ratio between the floating and the source region. Thus a higher coupling ratio can be provided as compared to the coupling ratio obtainable from the side diffusion of source implant.

It is clear that Lin et al. and the other cited references, taken either singly or collectively, failed to show or suggest the combination of claim elements of claim 14. As noted above and further emphasized, the present invention includes implanting first ions into the source region, followed by the deposition of a first polysilicon layer to form floating gates, and implanting second ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of the common source region. Lin et al. taught a completely different sequence of steps. Accordingly, claim 14 is also patentable over the cited references.

Claims 16 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14. Applicants respectfully disagree. Since claim 16 is dependant from independent claim 14, claim 16 is patentable for at least the reasons given above. Additionally, the cited references did not show or suggest the claim elements in claim 16, which recites that the first ions include N-type ions and the second ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted. Therefore, claim 16 is patentable over the cited art.

Having thus amended the application for clarification and having established that the cited references, taken either singly or collectively, failed to show or

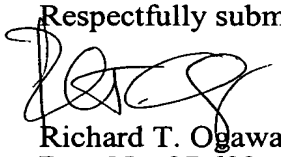
suggest the combination of claim elements of the claims in the present application, Applicants respectfully submit that the application is in condition for allowance. It is respectfully requested that rejection of claims 1 – 14 and 16 be reconsidered, and early notice thereof is solicited

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims a follows:

1. (Twice amended) A method of fabricating a flash memory device including an array of split gate cells, comprising the steps of:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each pair of said cells;

implanting ions into predefined areas **[on opposite sides]** of each said common source region;

forming **[pair of]** floating gates associated with **[each]** said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming **[a pair of]** drain regions associated with **[each]** said cells, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. (Once amended) A method for fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. (Once amended) A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. (Once amended) A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. (Twice amended) A method of fabricating a flash memory device as recited in claim 1, wherein said step of **[implanting ions]** forming floating gates includes the steps of:

forming a tunneling oxide layer over each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose first and second portions of said first polysilicon layer, said exposed first and second portions substantially define first and second floating gate regions; **[and]**

implanting ions into said first and second floating gate regions to adjust said threshold voltage; **[and**

wherein the forming of said pair of floating gates includes the steps of]

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, said remaining portions of said first polysilicon layer forming first and second floating gates associated with each said cell, said floating gates having side walls and a portion which overlies a portion of said common source region thereby providing a high coupling ration for the associated cell.

6. (Twice amended) A method of fabricating a flash memory device as recited in claim 1 **[5]** wherein said step of forming said select gates includes the steps of

forming an insulating layer over the exposed portion of said substrate and the floating gate oxide layer covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form said select gates.

7. (Once amended) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate and said floating gate oxide layer covering said floating gates includes the steps of

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. (Not amended) A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. (Not amended) A method of fabricating a flash memory device as recited in claim 1, wherein said ions include Boron ions.

10. (Once amended) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming drain regions associated with each cell includes the steps of

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and

implanting ions into said drain areas to form said drain regions.

11. (Once amended) A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region includes:

implanting arsenic ions to provide a dopant density in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV.

12. (Twice amended) A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C in order to form said first layer having a thickness in the range of 500 to 2500 angstroms.

13. (Not Amended) A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. (Once amended) A method of fabricating a flash memory device having a high coupling ratio, comprising the steps of

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating gate having side walls**[, having a portion which overlies a portion of said common source region thereby providing a high coupling ration for an associated cell]**;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer;

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates;

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least on drain area of said substrate; and

implanting third ions into said drain area of said substrate to form at least one drain region**[.]**;

whereby the floating gate having a portion which overlies a portion of said common source region thereby providing a high coupling ration for an associated cell.

16. (Twice amended) A method of fabricating a flash memory device as recited in claim 14, wherein said first ions include N-type ions and said second **[additional]** ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted.